Applicant(s)	Christopher J. Berens et al.	**PRELIMINARY AMENDMENT**
Serial No.	09/727,246	
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Title: CLOCK RECOVERY MECHANISM		

Commissioner for Patents
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Washington, D.C. 20231

Prior to taking up this application for examination, please amend the application as follows.

IN THE SPECIFICATION

Please delete the Brief Description of the Drawings on page 3, lines 17-28, and replace it with:

--Figure 1 is a flow chart diagram of a method according to one embodiment of the present invention;

Figure 2 is a flow chart diagram of a method according to another embodiment of the present invention;

Figure 2A is a flow chart diagram of another method according to the present invention;

Figure 3 is a block diagram of a transmit end of a system according to an embodiment of the present invention;

Figures 3A and 3B are more detailed block diagrams of the embodiment of Figure 3;

Figure 4 is a block diagram of a receive end of a system according to an embodiment of the present invention;

Figures 4A and 4B are more detailed block diagrams of the embodiment of Figure 4; and

Figure 5 is a block diagram of a telecommunications system according to an embodiment of the present invention.--

Please delete the last paragraph on Page 7, lines 26-31; Page 8, lines 1-6, and replace it with:

-- A front end transmit section of a system 300 is shown in block diagram in Figures 3, 3A, and 3B. In this embodiment, data is brought into the system at user data protocol interface 302, and presented to frequency estimator 304. In frequency estimator 304, the incoming data is converted from serial form to parallel form if necessary. Before flowing through the buffers 306 and related buffer circuitry 307, onto the system such as a local bus, PCI bus, or the like at system interface logic 308, frequency estimator 304 creates an estimate of the frequency of the incoming data stream as described above. The estimate is then encoded or embedded into the network traffic itself in ATM SAR logic 310. Logic 310 receives data 312 from the SRAM buffer 306 and frequency estimation data 314 from the estimation block 304, and embeds or appends the frequency estimation data into or with the data 312 to create ATM data containing both the data 312 and the frequency estimate 314.--

Please delete the second full paragraph on Page 8, lines 13-20 and replace it with:

-- In another embodiment, the receive end 400 of a system is shown in block diagram form in Figures 4, 4A, and 4B. In this embodiment, receive end 400 receives ATM network traffic 318 into system interface logic 402 and conveys the information to ATM SAR logic 404. In ATM SAR logic 404, the incoming data is separated to recover the frequency estimate bits from the data stream to provide the data 408 and the frequency estimate 410. The data 408 is presented to the SRAM buffer 406 and related buffer circuitry 407 and the frequency estimate 410 is presented to a clock recovery circuit 416.--

REMARKS

By this amendment, Applicant has substituted a new description of the drawings, and modified the specification. No new matter has been added. In the preparation of formal drawings, the original Figure 3 and the original Figure 4 were too large for reproduction on a single drawing sheet. Accordingly, they have been split into two sheets. The changes to the drawing description reflects those changes. The changes to the specification make proper reference to the split Figures 3 and 4.

Respectfully submitted,

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MARKED-UP VERSIONS OF AMENDMENTS

IN THE SPECIFICATION

Brief Description of the Drawings on page 3, beginning at line 17:

Figure 1 is a flow chart diagram of a method according to one embodiment of the present invention;

Figure 2 is a flow chart diagram of a method according to another embodiment of the present invention;

Figure 2A is a flow chart diagram of another method according to the present invention;

Figure 3 is a block diagram of a transmit end of a system according to an embodiment of the present invention;

Figures 3A and 3B are more detailed block diagrams of the embodiment of Figure 3;

Figure 4 is a block diagram of a receive end of a system according to an embodiment of the present invention; [and]

Figures 4A and 4B are more detailed block diagrams of the embodiment of Figure 4; and

Figure 5 is a block diagram of a telecommunications system according to an embodiment of the present invention.

Last paragraph on Page 7, beginning at line 26:

A front end transmit section of a system 300 is shown in block diagram in [Figure 3] Figures 3, 3A, and 3B. In this embodiment, data is brought into the system at user data protocol interface 302, and presented to frequency estimator 304. In frequency estimator 304, the incoming data is converted from serial form to parallel form if necessary. Before flowing through the buffers 306 and related buffer circuitry 307, onto the system such as a local bus, PCI bus, or the like at system interface logic 308, frequency estimator 304 creates an estimate of the frequency of the incoming data stream as described above. The estimate is then encoded or embedded into the network traffic itself in ATM SAR logic 310. Logic 310 receives data 312 from the SRAM buffer 306 and frequency estimation data 314 from the estimation block 304, and embeds or appends the frequency estimation data into or with the data 312 to create ATM data containing both the data 312 and the frequency estimate 314.

Second full paragraph on Page 8, beginning at line 13:

-- In another embodiment, the receive end 400 of a system is shown in block diagram form in [Figure 4] Figures 4, 4A, and 4B. In this embodiment, receive end 400 receives ATM network traffic 318 into system interface logic 402 and conveys the information to ATM SAR logic 404. In ATM SAR logic 404, the incoming data is separated to recover the frequency estimate bits from the data stream to provide the data 408 and the frequency estimate 410. The data 408 is presented to the SRAM buffer 406 and related buffer circuitry 407 and the frequency estimate 410 is presented to a clock recovery circuit 416.